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Mullins

PATENT
Attorney Docket No. 70803

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
David Glen Roe

Application No. 09/814,244

Filed: March 21, 2001

Group Art Unit: 2816

Examiner: COX, CASSANDRA F.

For: METHOD AND APPARATUS FOR PROVIDING MULTIPLE CLOCK SIGNALS ON A CHIP USING A SECOND PLL LIBRARY CIRCUIT CONNECTED TO A BUFFERED REFERENCE CLOCK OUTPUT OF A FIRST PLL LIBRARY CIRCUIT

CERTIFICATE OF MAILING

I hereby certify that this paper is being deposited with the United States Postal Service on the date shown with sufficient postage as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, **on March 24, 2003.**

3/24/03
Kirk D. Williams, Esq.

RESPONSE B

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

In response to the non-final Office action mailed December 24, 2002, please consider the following remarks. Reconsideration and/or further prosecution of the application is respectfully requested.

The Office action dated December 24, 2002, and the references cited therein have been carefully considered. Applicants traverse all rejections for at least the reasons stated herein after. Moreover, applicant requests allowance of all claims as the prior art of record neither teaches nor suggests the invention recited in the pending claims.

Applicant encourages the Office to contact and discuss this case with the undersigned attorney to help move this application along to allowance.

The following remarks reference the same numbered paragraphs of the Office action to which they are directed.

Paragraph 3. Claims 1, 9, 15, 18, and 20 (all five pending independent claims) stand rejected under 35 USC 102(b) as being anticipated by Saeger et al., US Patent 5,565,928.

Applicants traverse these rejections as the Office action fails to establish a *primia facie* case of anticipation as Saeger et al. fails to show each and every element of the claim as required. *See*, MPEP § 2131 and 35 USC § 102.

As to claim 1, first, Saeger et al. fails to disclose a buffered reference clock output. The Office action cites signal 167 as a buffered reference clock output. Signal 167 is the output of the phase-locked loop circuitry (58, 68, 34, 142, 44, 160) cited in the Office action. A buffered reference clock output is an non-inverted or inverted representation of the clock input signal. Specification, at least on p. 10, ll. 4-6. Clearly, signal 167 is not an non-inverted or inverted representation of Saeger et al.'s clock input signal 26. Rather, signal 167 appears to be a phase-locked loop output (which corresponds to a different element of claim 1). For at least this reason, Saeger et al. fails to anticipate claim 1. Moreover, Saeger et al. neither teaches nor suggests a buffered reference clock output.

Moreover, the Office action cites Saeger et al's signal 32 as a first set of one or more phase locked loop clock outputs. Applicant does not see how Saeger et al.'s "triggering signal 32" is an output of the phase-locked loop circuitry (58, 68, 34, 142, 44, 160), rather it is the counted down output 32 of divide-by-16 counter 74. In contrast, claim 1 recites "a first set of one or *more phase-locked loop clock outputs*," not an internal signal of the phase-locked loop circuitry (58, 68, 34, 142, 44, 160). Rather, signal 167 appears to be a phase-locked loop output. For at least this reason, Saeger et al. fails to anticipate claim 1.

To the extent appropriate, this same rational applies to claims 9, 15, 18, and 20.

Moreover, the Office action fails to comply with the MPEP as it fails to present a rejection for each and every element. For example, claim 9 recites "means for buffering a

received off-chip reference clock signal electrically coupled between the off-chip reference clock input and the buffered reference clock output," claim 15 recites "selecting a first phase-locked loop macro..." and "selecting a second phase-locked loop macro...," and claim 20 recites "means for generating, by the first phase-locked loop circuit, a buffered reference clock signal and the first set of internal clock reference signals." These elements/limitations are neither taught nor suggested by the prior art of record, and for at least these reasons, are believed to be allowable. Applicant requests the Office action either allow a claim or provide a specific rejection and a cited teaching for each and every claim element/limitation and each and every recited combination of elements/limitations as required by the MPEP.

As the Office action fails to present a *prima facie* case of anticipation or obviousness in conformance with the MPEP, all five independent claims 1, 9, 15, 18, and 20, and their dependent claims 2-8, 10-14, 16-17, and 19 are believed to be allowable.

Paragraph 5. Claims 2-8, 10-14, 16-17, and 19 stand rejected under 35 USC 103(a) as being obvious over Saeger et al., US. Patent 5,565,928, in view of the "Phase-Locked Loop" IBM reference ("IBM reference").

Applicants traverse these rejections as the Office action fails to establish a primia facie case of obviousness as Saeger et al., alone or in combination with the IBM reference, neither teaches nor suggests all the claim elements and limitations as required by the MPEP. The burden is on the Office Action to establish a prima facie case of obviousness, which has not been done as the MPEP requires, *inter alia*, that:

> "the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure."

MPEP § 706.02(j) (*citing In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991))(emphasis added).

First, for at least the reasons presented herein in relation to Paragraph 3, the Office action fails to make a prima facie case of anticipation nor obviousness in regards to all pending independent claims, and thus, all pending claims (claims 1-20) are believed to be allowable as the rejections in relation to Paragraph 5 rely on such a prima facie case being established.

Next, there is no teaching to combine Saeger et al. with the IBM reference.

First, Applicant agrees with the July 17, 2002, Office action that the "IBM reference does not disclose that the buffered reference clock output (BUFREFCLK) of the first phase-locked loop circuit is electrically coupled to the on-chip reference clock input (REFCLK) of the second phase-locked loop circuit (PLL7SLIBI)." Moreover, applicants submit that the IBM reference teaches away from such a combination as recited in independent claim 1. The IBM Reference, at least on page 843, teaches that the REFCLK of PLL7SLIBI "typically connects to the output of a receiver. Any receiver in the library may be used (differential or single-ended) provided that it is located in a test I/O slot." In other words, the IBM reference teaches that the REFCLK of PLL7SLIBI is connected to an I/O receiver (e.g., for receiving an off-chip signal), and not to another component, such as BUFREFCLK of a first phase-locked loop circuit. Saeger et al. provides no teaching to overcome this deficiency.

Moreover, even if there was such a teaching, the combination of Saeger et al. with the IBM reference produces a circuit with the on-chip reference clock input of a second phase-locked loop circuit *coupled to one output of a first set of one or more phase-locked loop clock outputs of a first phase-locked loop circuit.* In contrast, claims 1-20 require the on-chip reference clock input of a second phase-locked loop circuit to be *coupled to the buffered reference clock output of a first phase-locked loop circuit.* For at least this reason, Saeger et al. nor the IBM reference, alone or in combination, neither teaches nor suggests the invention recited in claims 1-20.

For at least these reasons, applicants request the rejections of claims 1-20 be withdrawn, and claims 1-20 be allowed.

CONCLUSION

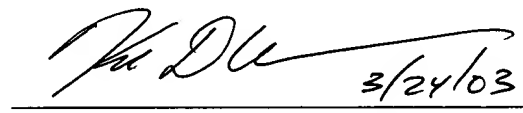
In view of the above remarks, the application is considered in good and proper form for allowance, and the Examiner is respectfully requested to pass this application to issue. If, in the opinion of the Examiner, a telephone conference would expedite the prosecution of the subject application, the Examiner is invited to call the undersigned attorney.

The Commissioner is hereby generally authorized under 37 C.F.R. § 1.136(a)(3) to treat this communication or any future communication in this or any related application filed pursuant to 37 C.F.R. § 1.53 requiring an extension of time as incorporating a request therefore, and the Commissioner is hereby specifically authorized to charge Deposit Account No. 501430 for any fee that may be due in connection with such a request for an extension of time.

The Commissioner is hereby authorized to charge payment of any fee due any under 37 C.F.R. §§ 1.16 and § 1.17 associated with this communication or any future communication in this or any related application filed pursuant to 37 C.F.R. § 1.53 or credit any overpayment to Deposit Account No. 501430.

Respectfully submitted,
The Law Office of Kirk D. Williams

Date: March 24, 2003

By  3/24/03

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